Appl. No. 10/707,175
Amdt. Dated 08/03/2005
Reply to Office action of 05/03/05

REMARKS/ARGUMENTS

This is in response to the Office Action dated May 3, 2005

Status of Claims/Other

Claims 1-25 are pending.

Claims 1-14 are rejected.

Claims 15-25 are withdrawn from consideration.

The drawing status is.... not specified.

Election/Restrictions

Applicant's election without traverse of Group I, claims 1-14 in the reply filed on 4/15/05 is acknowledged.

Claims 15-25 are withdrawn from further consideration by the examiner, 37 C.F.R. 1.142(b) as being drawn to a non-elected invention. Election was made without traverse.

Claims 15-25 are canceled herewith.

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

A new title is provided herewith.

Claim Objections

Claim 1 is objected to because of the following informalities: in claim 1, line 13, there is a typographical error, it is suggested to delete "and". Appropriate correction is required.

The word "to" has been removed.

Claim Rejections - 35 USC 102

<u>**Claims 1, 7, 12-14** are rejected under 35 U.S.C. 102(e) as being anticipated by Murthy et al (U.S. Patent No. 2004/0007724).</u>

Referring to figures 7-14, Murthy et al. teaches a method of forming a semiconductor device, comprising:

providing a semiconductor structure comprising a silicon substrate (12) and a gate structure (22) formed on the silicon substrate, the gate structure further comprising a gate contact (14) and a gate insulator(18, see figure 7, 14, paragraph# 26);

selectively forming etched-away areas (40) in the substrate to expose sides of a channel region under the gate structure (see figure 7, paragraph# 36);

disposing a thin, highly-doped layer (52) of a silicidation stop material (SiGe) within the etched a-way areas (40, see paragraph # 45);

disposing a silicon fill (56) within the etched-away areas over a silicidation stop the silicidation stop material to; and (see paragraph# 44-49)

performing silicidation to form silicide in the silicon fill, thereby forming source/drain silicide regions (74, see figure 14, paragraphs 52-54).

Regarding to **claim 7**, the silicidation stop material is in-situ doped (see paragraph# 45).

Regarding to **claim 12**, the semiconductor structure is an inchoate n-channel MOSFET
(see paragraphs# 24, 56).

Regarding to **claim 13**, the semiconductor structure is an inchoate p-channel MOSFET (see paragraphs# 24, 56).

Regarding to **claim 14**, the semiconductor structure is part of an inchoate CMOS device (see paragraphs# 24, 56, noted that CMOS is NMOS+PMOS).

Claim Rejections - 35 USC 103

<u>**Claims 2-6, 8-11** are rejected under 35 U.S.C. 103(a) as being unpatentable over Murthy et al. (U.S. Patent No. 2004/0007724) as applied to claims 1, 7, 12-14 in view of ordinary skill in the requisite art.</u>

Murthy et al. teaches a method of forming a semiconductor device with forming a highly doped layer of a silicidation stop material SiGe (see paragraph 45, meeting claim 3), forming a silicide cobalt (see paragraph# 52, meeting claim 4), the active dopant concentration is greater than 1019 atoms/cm3 (paragraph# 46, meet claim 10) wherein the silicidation temperature is about 400-500oC (see paragraph# 54), and forming ultra thin SiGe layer (see paragraph# 45). However, the reference does not teach the specific silicidation temperature, and the thickness of the silicidation-stop extensions.

It would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to optimize the specific silicidation temperature, and the thickness of the silicidation-stop extensions, since it has been held that where the general conditions of a claim are disclosed in the prior art (i.e.-hydrogenated dielectric layer), discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233 (CCPA 1955).

The specification contains no disclosure of either the critical nature of the claimed arrangement (i.e. - wherein the specific silicidation temperature, and the thickness of the silicidation-stop extensions.) or any unexpected results arising there from. Where patentability is said to be based upon particular chosen limitations or upon another variable recited in a claim, the applicant must show that the chosen limitations are critical. In re Woodruff 919 F.2d 1575, 1578 (FED. Cir. 1990).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would form the suicide film at a specific silicidation temperature in order to optimize the process and forming a silicidation-stop extensions at a specific thickness in order to obtain the smaller dimension device.

The Invention, Generally

The present invention relates to semiconductor device manufacturing and processing techniques, and more particularly to the formation of lateral extensions in metal oxide semiconductor field effect transistors (MOSFETs).

Generally, the invention provides a structure and method for reliably forming thin, highly-doped layers between source/drain silicide and a MOSFET channel region without risk of breach by the silicide.

Very low resistance, scaled in MOSFET devices are formed by employing thin silicidation-stop extension that act both as a silicidation "stop" barriers and as thin interface layers between source/drain silicide regions and channel region of the MOSFET. By acting as silicidation stops, the silicidation-stop extensions confine silicidation, and are not breached by source/drain silicide. This permits extremely thin, highly-doped silicidation-stop extensions to be formed between the silicide and the channel, providing an essentially ideal, low series resistance interface between the silicide and the channel. On an appropriately prepared substrate, a selective etching process is performed to expose the sides of the channel region (transistor body). A very thin layer of a silicidation-stop material, e.g., SiGe, is disposed in the etched away area, coating the exposed sides of the channel region. The silicidation-stop material is doped (highly) appropriately for the type of MOSFET being formed (n-channel or p-channel). The etched away areas are then filled with silicon, e.g., by a Si epi process. Silicidation is then performed (to form, e.g., $CoSi_2$) on the newly filled areas. The silicidation stop material constrains silicidation to the silicon fill material, but prevents silicide expansion past the silicidation stop material. Because the germanium (Ge) in SiGe is insoluble in $CoSi_2$, the SiGe acts as a barrier to silicidation, permitting silicidation to go to completion in the Si fill but stopping silicidation at the SiGe boundary when silicidation is performed at a temperature above a silicidation threshold temperature for Si, but below a silicidation threshold temperature for SiGe. This results in a very compact, well-defined lateral junction characterized by a thin layer of SiGe disposed between silicide lateral extensions and the sides of the channel region. Because of the thin, highly-doped SiGe layer between the channel and the silicide lateral extensions, the extension resistance is very low.

Traversing the Rejections

US20040007724 ("Murthy") discloses a version of a raised source/drain (RSD) structure. RSD structures are widely known in the transistor art and are typically employed for ultra-thin body SOI devices (SOI thickness of less than about 500A, see, for instance, paragraph [0029] of Murthy) to reduce series resistance of a thin source/drain region. Murthy augments a typical RSD structure with a lowered epitaxial region self-aligned to the gate edge and formed by semi-isotropic reactive ion etch process such that the amount of gate edge undercut is controlled via the degree of isotropicity of such reactive ion etch process.

Murthy does not teach a multilayered epitaxial structure that, in the combination with a specific silicide material and related silicidation process, provides an ultra-thin silicidation barrier (or silicidation stop layer) and allows for placing a highly conductive metallic silicide layer in the close proximity of transistor channel without any direct contact with the transistor body.

The present invention teaches a field effect transistor with a multilayered epitaxial structure (refer to **FIG. 4**, layers 120 and 122) where the first layer (120) comprises the first epitaxial material (silicidation-stop extensions) and the second layer (122) comprises the second silicon-containing material (which is silicided). The property of the first epitaxial material 120 is such that it reacts very slowly (or does not react at all) with refractory metal atoms employed in the silicidation process. The property of the second silicon-containing material 122 is such that it readily and quickly reacts with the refractory metal atoms forming a highly conductive silicide layer (124) as shown in **FIG. 5** and described in paragraph [0064].

Although the term "multilayer" is not specifically used in the specification with respect to the layers 120 and 122, it's meaning is self-evident, and it is used in other instances throughout the specification in its conventional sense to describe other "multilayer" structures, such as the substrate 102 which "may comprise a multilayer structure in which at least the top layer thereof is semiconducting and, preferably, is silicon."

To the contrary, Murthy teaches a transistor structure with a single epitaxial layer 52 (see, for example, FIG. 8 through FIG. 14) that readily reacts with refractory metal atoms forming a silicide layer 74 as shown in FIG. 13 and FIG. 14 and described in paragraph [0052].

The present invention further teaches a useful range of layer 120 thickness of from about 10A to about 100A as described in paragraphs [0038], [0039], [0066]. The thickness of layer 120 sets the separation between the highly conductive silicide layer 124 and the transistor channel 128 as shown in **FIG. 7**.

To the contrary, Murthy teaches that the edge of silicide layer 74 is separated from the transistor body/channel 36 via a set of spacers 26, 28, 66 as shown in FIG. 14. Murthy further teaches in

paragraphs [0029], [0049] and [0050] that the thickness range of the set of spacers 26, 28, 66 is from about 550A to about 2600A.

The present invention further teaches in paragraph [0037] the use of Si:C material (silicon doped with carbon) as layer 120 when the silicide layer 124 is nickel silicide (NiSi), for instance.

Murthy does not teach the use of Si:C.

The present invention further teaches in paragraph [0055] the use of crystallographic-plane-dependent etch for a controllable undercut. While the etch rate may vary the angle of slow etching crystallographic plane is fixed by the crystalline structure. Further, the slow etching (111) plane of silicon is very stable against unwanted oxidation at the ambient temperature thus reducing amount of interfacial defects.

Murthy does not teach the use of crystallographic-plane-dependent etch for a controllable undercut.

In the present invention, the recessed regions 114, 116 extend into the surface of the substrate, and are therefore below the surface of the substrate. The recessed regions (also called "recessed areas") are then filled with two layers - first thin silicidation-stop extensions 120 on either side of the channel region 118, then silicon fill material 122 which is silicided (124). [0066] By the inventive technique described hereinabove with respect to Figures 1-5, the silicidation-stop extensions can made be extremely thin, e.g., (10-100Å SiGe under 300Å thick $CoSi_2$ source/drain silicide) while remaining resistant to breach (in the manner described hereinabove) by the silicidation process.

The result is that the two (multi) layers of material disposed in the recesses is also below (or even with) the surface of the substrate 102. This is not taught or suggested by Murthy.

Claim 1 is amended to include subject matter from paragraph [0061] ...

[0061] Figure 4 shows a structure 400 resulting from filling etched away areas 114 and

116 over the silicidation-stop extensions 120. Silicon fill regions 122 now completely fill the etched away areas 114 and 116 (see Fig. 2) over the thin silicidation-stop extensions 120, thereby interposing the thin silicidation-stop extensions 120 between the Si fill regions 122 and the channel region 118 (and the substrate 102).

Accordingly, claim 1 should be allowed.

Claims 2-14 and 26-28 depend upon claim 1 and should also be allowable.

The newly presented claims are supported by the text of the specification.

The claim count does not exceed 20 total claims, 3 independent.

Conclusion

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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